

**WEST****Freeform Search****Database:**

US Patents Full-Text Database  
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 Derwent World Patents Index  
 IBM Technical Disclosure Bulletins

**Term:**
**Display:**  **Documents in Display Format:**  **Starting with Number** 
**Generate:** ☐ Hit List ☒ Hit Count ☐ Side by Side ☐ Image

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Cases

**Search History**
**DATE:** Monday, April 21, 2003    [Printable Copy](#)    [Create Case](#)
**Set Name Query**

side by side

**Hit Count Set Name**

result set

*DB=USPT; PLUR=YES; OP=ADJ*

<u>L8</u>	L7 and (bus near8 (clock adj rate))	8	<u>L8</u>
<u>L7</u>	L6 and (memory near4 control\$4)	109	<u>L7</u>
<u>L6</u>	L5 and (interface near8 (bit or byte))	119	<u>L6</u>
<u>L5</u>	l3 and l4	350	<u>L5</u>
<u>L4</u>	((memory or external) near4 bus) near8 (width or wide or bandwidth)	2346	<u>L4</u>
<u>L3</u>	((SIMM or DIMM or (memory adj module) or internal) near4 bus) near8 (width or wide or bandwidth)	796	<u>L3</u>
<u>L2</u>	(SIMM or DIMM or (memory adj module) or internal) near8 (width or wide or bandwidth)	12704	<u>L2</u>
<u>L1</u>	(SIMM or DIMM or module or internal) near8 (width or wide or bandwidth)	20314	<u>L1</u>

END OF SEARCH HISTORY

**Set Name Query**

side by side

**Hit Count Set Name**

result set

*DB=USPT; PLUR=YES; OP=ADJ*

<u>L24</u>	L10 and (point adj2 point)	1	<u>L24</u>
<u>L23</u>	L10 (point adj2 point)	0	<u>L23</u>
<u>L22</u>	l21 and strobe	1	<u>L22</u>
<u>L21</u>	L6 and (internal or external) and (register or latch\$4)	2	<u>L21</u>
<u>L20</u>	L6 and strobe and (register or latch\$4)	1	<u>L20</u>
<u>L19</u>	L11 and ((port or link) near8 (point adj2 point))	0	<u>L19</u>
<u>L18</u>	L11 and ((DIMM or SIMM or module) near8 (point adj2 point))	1	<u>L18</u>
<u>L17</u>	L10 and ((DIMM or SIMM or module) near8 (point adj2 point))	1	<u>L17</u>
<u>L16</u>	L14 and (port near8 (DIMM or SIMM or module) near8 (point adj2 point))	0	<u>L16</u>
<u>L15</u>	L14 and (port near8 (point adj2 point))	7	<u>L15</u>
<u>L14</u>	L13 and (port near8 (DIMM or (memory adj2 module)))	66	<u>L14</u>
<u>L13</u>	module near8 ((buffer or register) near4 port)	353	<u>L13</u>
<u>L12</u>	L11 and ((buffer or register) near4 port)	0	<u>L12</u>
<u>L11</u>	L10 or l6	6	<u>L11</u>
<u>L10</u>	(6530033 or 5815646 or 6141739 or 5825424).pn.	4	<u>L10</u>
<u>L9</u>	L6 and interface and strobe and (signal\$3 adj2 line)	1	<u>L9</u>
<u>L8</u>	L6 and board and print\$3 and connect\$3	2	<u>L8</u>
<u>L7</u>	L6 and board	2	<u>L7</u>
<u>L6</u>	(6034878 or 6169687).pn.	2	<u>L6</u>
<u>L5</u>	(DIMM or ((dual or double) adj4 module)) near6 board near8 (connect\$4 near4 bus)	3	<u>L5</u>
<u>L4</u>	(DIMM or module) near6 board near8 (connect\$4 near4 bus)	183	<u>L4</u>
<u>L3</u>	(bus near4 (clock or rate)) near8 (rank or bank) near8 (factor or ratio or "1/R" or "1/N")	0	<u>L3</u>
<u>L2</u>	(bus near4 (clock or rate)) near8 (register or device) near8 (factor or ratio or "1/R" or "1/N")	15	<u>L2</u>
<u>L1</u>	(ring near4 bus) near8 (DIMM or (memory adj module)) near8 (control\$4 or arbit\$8)	1	<u>L1</u>

END OF SEARCH HISTORY